CLAIMS

What is claimed is:

1. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside, wherein a circuit density of a ratio of total cell area to total available site area can be one hundred percent;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area.

2. The method of Claim 1, wherein said detailed placement process runs in linear time.

3. The method of Claim 1, wherein said detailed placement process uses a subroutine that improves placement by swapping cells between pairs of rows.

4. The method of Claim 3, wherein said detailed placement process further comprises the step of using a dynamic programming technique to perform the swapping of cells.

5. The method of Claim 3, wherein a lookahead parameter is used to control usages of row swapping.

6. The method of Claim 4, wherein said detailed placement process further comprises the step of pruning a search space during said dynamic programming process.

7. The method of Claim 6, wherein said pruning step is controlled as a function of a gap count.

8. The method of Claim 1, wherein said detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

9. The method of Claim 1, wherein said detailed placement process further comprises the step of assigning an initial cell location based on a result of said coarse placement process.

10. The method of Claim 9, wherein said coarse placement process uses a conjugate gradient method.

11. The method of Claim 9, wherein said detailed placement process further comprises the step of optimizing a y-location of said cells during said initial phase of cell location assignment.

12. The method of Claim 11, wherein said optimizing step is performed through said dynamic programming technique.

13. The method of Claim 12, wherein said detailed placement process further comprises the step of performing a greedy cleanup phase.

14. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a dynamic programming technique to perform a swapping of cells.

15. The method of Claim 14, wherein said detailed placement process runs in linear time.

16. The method of Claim 14, wherein said detailed placement process uses a subroutine that improves placement by swapping cells between pairs of rows.

17. The method of Claim 14, wherein a circuit density of a ratio of total cell area to total available site area can be one hundred percent.

18. The method of Claim 16, wherein a lookahead parameter is used to control usages of row swapping.

19. The method of Claim 14, wherein said detailed placement process further comprises the step of pruning a search space during said dynamic programming process.

20. The method of Claim 19, wherein said pruning step is controlled as a function of a gap count.

21. The method of Claim 14, wherein said detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

22. The method of Claim 14, wherein said detailed placement process further comprises the step of assigning an initial cell location based on a result of said coarse placement process.

23. The method of Claim 22, wherein said coarse placement process uses a conjugate gradient method.

24. The method of Claim 22, wherein said detailed placement process further comprises the step of optimizing a y-location of said cells during said initial phase of cell location assignment.

25. The method of Claim 24, wherein said optimizing step is performed through said dynamic programming technique.

26. The method of Claim 25, wherein said detailed placement process further comprises the step of performing a greedy cleanup phase.

27. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells according to a conjugate gradient process;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area.

28. The method of Claim 27, wherein said detailed placement process runs in linear time.

29. The method of Claim 27, wherein said detailed placement process uses a subroutine that improves placement by swapping cells between pairs of rows.

30. The method of Claim 29, wherein a circuit density of a ratio of total cell area to total available site area can be one hundred percent.

31. The method of Claim 29, wherein a lookahead parameter is used to control usages of row swapping.

32. The method of Claim 30, wherein said detailed placement process further comprises the step of pruning a search space during said dynamic programming process.

33. The method of Claim 27, wherein said pruning step is controlled as a function of a gap count.

34. The method of Claim 27, wherein said detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

35. The method of Claim 34, wherein said detailed placement process further comprises the step of assigning an initial cell location based on a result of said coarse placement process.

36. The method of Claim 35 further comprising the step of using a dynamic programming technique to perform a swapping of cells.

37. The method of Claim 35, wherein said detailed placement process further comprises the step of optimizing a y-location of said cells during said initial phase of cell location assignment.

38. The method of Claim 37, wherein said optimizing step is performed through said dynamic programming technique.

39. The method of Claim 38, wherein said detailed placement process further comprises the step of performing a greedy cleanup phase.

40. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes a single row optimally according to a sum of squares objective in linear, quadratic, or polynomial run time.

41. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes a single row optimally for a given fixed cell ordering in linear, quadratic, or polynomial run time.

42. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

legalizing a single row optimally using a dynamic programming technique.

43. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes two rows optimally according to a sum of squares objective in quadratic or polynomial run time.

44. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes two rows optimally for a given fixed cell ordering in quadratic or polynomial run time.

45. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

legalizing two rows optimally using a dynamic programming technique.

46. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes a pair of rows optimally according to a y-displacement metric in quadratic or polynomial time.

47. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site

boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes N rows optimally according to a y-displacement metric in quadratic or polynomial time.

48. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes one or more rows optimally according to a y-displacement metric, is polynomial in a number of sites, and runs in time polynomial in the number of sites.

49. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes N rows optimally according to a sum of squares objective and which runs in time polynomial in the number of sites.

50. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes N rows optimally according to a sum of squares objective and which runs in time polynomial in the number of sites.

51. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells according to a non-linear programming optimization algorithm;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area.

52. The method of Claim 51, wherein said non-linear programming optimization algorithm includes one of conjugate gradient, quasi-newton, partial newton, or full newton.

53. A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells according to a conjugate gradient or quasi-newton process;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area in non-quadratic and non-linear run times.

54. A computer-readable medium having stored thereon instructions for placing cells of a netlist comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside, wherein a circuit density of a ratio of total cell area to total available site area can be one hundred percent;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area.

55. A computer-readable medium having stored thereon instructions for placing cells of a netlist comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group

of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a dynamic programming technique to perform a swapping of cells.

56. A computer-readable medium having stored thereon instructions for placing cells of a netlist comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells according to a conjugate gradient process;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area.

57. A computer-readable medium having stored thereon instructions for placing cells of a netlist comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells;

performing a detailed placement process which assigns a final location to each of said cells, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that said each cell can be placed on said legal sites without violating constraints set forth in said specification of said placement area;

using a subroutine that legalizes a single row optimally according to a sum of squares objective in linear, quadratic, or polynomial run time.